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10EC021

M.Tech. Degree Examination, January 2011
CMOS VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Describe the construction, working and characteristics of enhancement mode MOSFET, with the relevant figure. Compare the characteristics of this MOSFET with depletion mode MOSFET. **(10 Marks)**

b. Define the body effect in MOSSEFT. Derive the MOSFET current equation, in different regions of operation. **(10 Marks)**

2 a. Explain the working of BICMOS inverter. State how the stored charges in the base are eliminated. Write the circuit diagram of BICMOS NAND gate. **(10 Marks)**

b. Describe the term tunneling and punch through in MOSFET. **(04 Marks)**

c. Briefly explain the pseudo nMOS inverter and the saturated load inverter, with their output characteristics. **(06 Marks)**

3 a. What is meant by lamda based design rules? List the lamda based design rules for metal layer, polysillicon layer and transistor. **(08 Marks)**

b. Describe with a neat sketch, pwell process for CMOS fabrication. **(08 Marks)**

c. Derive the scaling factors for the following CMOS parameters :
i) Gate capacitance C_g ii) Gate delay T_d **(04 Marks)**

4 a. Explain the sheet resistance and standard unit capacitance. What is the effect of fluse parameter in delay unit 7? **(10 Marks)**

b. Bring out the difference stick diagram and layout. Draw the schematic and layout diagram for the following functions.
i) $Y = \overline{A + \overline{B}C}$ ii) $Y = AB + \overline{A}\,\overline{B}$. **(10 Marks)**

5 a. Explain the effect of parasitic capacitance in CMOS 2 input NOR gate. **(04 Marks)**

b. Prove that the switching threshold of NOR2 is $V_{DD}/2$, when $U_{tn} = |U_{tp}|$ and $k_p = UK_n$. **(06 Marks)**

c. By constructing Euler graph, for the pull up and pull down device, draw the stick diagram for following logic function.
$Z = \overline{A(D+E)+BC}$.
Also draw the optimized stick diagram for the same. **(10 Marks)**

6 a. Describe the behavior of bistable element. Derive the expression for the output voltage. **(08 Marks)**

b. What is clocked latch? Write and explain AOI based implementation of the clocked NOR based SR latch. **(08 Marks)**

c. Draw the dynamic CMOS logic and explain the pre-charge and evaluation mode. **(04 Marks)**

7 a. What is pass transistor? Describe how does logic '0' transfer and logic '1' transfer takes place in pass transistor. **(10 Marks)**

b. Explain the different types of current mirror circuits. How can these be used in the design of a differential amplifier? **(10 Marks)**

8 Write short notes on :
a. Differential inverter
b. Complementary pass logic
c. Domino logic
d. Inpact ionization in MOS transistors. **(20 Marks)**

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10EC116

M.Tech. Degree Examination, January 2011

Advanced Microcontrollers

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Explain the trade-offs of a low power embedded systems with the of cortex MS. **(10 Marks)**

b. Describe von-Neumann architecture and Harvard architecture. Compare them with the help of a neat diagram. **(10 Marks)**

2 a. With a neat block diagram, explain the architecture of MSP 430. **(12 Marks)**

b. List and briefly explain the characteristics of MSP 430 microcontrollers. **(08 Marks)**

3 a. With the help of a neat block diagram, explain MSP 430 CPU. Also explain the functions of dedicated registers. **(12 Marks)**

b. Explain the 3 – core instruction with its format with emulation. **(08 Marks)**

4 a. Explain 16 bit WDT module, used as process or supervisor and internal timer. **(10 Marks)**

b. Describe low power operating modes, supported by the MSP 430 architecture. Explain the rules of thumb configuration of low power applications. **(10 Marks)**

5 With the help of a neat diagram, explain cortex M3. **(20 Marks)**

6 a. Explain the assemble language with basic syntax, unified assemble language and use of suffixes, with an example. **(10 Marks)**

b. Explain with a neat figure the priority levels of cortex M3, using 3 bit or 4 bit priority width, for exceptional programming. **(10 Marks)**

7 a. Explain the occurrence of interrupts or exception sequences in detail, with a neat diagram. **(10 Marks)**

b. Explain the functions associated with external interrupt, having several registers and interrupt processing. **(10 Marks)**

8 Write short notes on : **(20 Marks)**

a. Wireless sensor network and MSP 430

b. Pulse width modulation in power supplies

c. Interrupt sources in MSP 430

d. Frequency locked loop in MSP 430.

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